AMENDMENTS TO THE SPECIFICATION:

Please amend the specification as follows.

At page 2, lines 13-26:

As described above, according to the prior art, when the main clock is stopped for some cause, the stop is dealt with by switching the main clock to the sub clock and there is not provided a constitution of spontaneously issuing a reset signal and initializing the clock as in the present invention. Therefore, when the main clock is stopped, the main clock is switched to the sub clock which continues operating in a state as it is and there is a drawback that in order to recover an original state, a control or the like by a software is separately needed. Further, since the normally-counted signal is the sub clock, much time is needed until the counter overflows, as a result, there also poses a problem of producing time lag until the stop is dealt ~~deal~~ with (switch to sub clock). When the sub clock is stopped, the abnormal stop cannot be detected.

At page 6, line 24, to page 7, line 14:

The main clock monitoring circuit 401 counts a main clock by the included counter and issues a normal operation confirming flag no_reset constituting "H" ("1", that is, signifying high level) indicating that normal operation is being carried out when the ~~then~~ counter is equal to a predetermined set value, or overflowed. The flag no_reset is monitored at fall of a sub clock. The reset_A1 flag generating circuit 402 issues a flag reset_A1 constituting "H" when the no_reset is "H" and "L" when the no_reset is "L" ("0", that is, signifying low level). The reset_A2 flag generating circuit 403 issues a main clock stop flag reset_A2 inverting the flag reset_A1 and delaying by a half period of the sub clock and issues a main clock initializing

(main microcomputer resetting) signal. However, the reset_A2 flag generating circuit 403 issues the signals only when the main clock is determined to stop. When the main clock is recovered by receiving the main clock initializing signal, the reset_A2 flag generating circuit 403 continues operating as it is by resetting the main clock stop flag reset_A2.